AMENDMENT TO THE CLAIMS

This listing of claims replaces all prior listings of claims.

1. Canceled

2. (Currently amended) An application specific coprocessor system for use with a processor for use in massive data manipulations specific to an application and adapted for attachment to a workstation having a general purpose processor, said coprocessor system having programming code which is assembled as instructions for said specific application in combination with accelerator environment specific requirements, independently provided, wherein

said environment specific instructions are accessed by a compiler in response to user input in an application specific form; and

wherein said compiler comprises:

a user interface to permit an application trained non circuit design trained user to enter instructions to achieve application specific accelerated processing;

means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs; and

means for identifying bit demands for the application specific accelerated processing needs such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives.

3. Canceled

4. (Currently amended) The coprocessor of ~~claim 3~~ claim 2 wherein said compiler comprises one or more of: ~~user interface to permit an application trained non circuit design trained user to enter instructions to achieve accelerated performance, means to create an internal~~

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~~representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs, means for identifying bit demands for the application specific coprocessor acceleration function,~~ mapper means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing, balancing means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

5. (Original) The coprocessor of claim 4 wherein said mapper means accepts as input domain specific policy information, estimates of the amount of logic needed for each processing element, and hardware context information that states what amounts of each logic resource exist on a given coprocessor to enable the largest possible number of processing elements said coprocessor can support.

6. (Original) The coprocessor of claim 5 wherein said balancing means analyzes the processing speed of said coprocessor at each step and allocates parallel hardware in proportion to a speed requirement.

7. (Currently Amended) The coprocessor of ~~claim 3~~ claim 2 wherein said compiler further ~~includes~~ comprises one or more of: prerecorded ~~information; reflecting~~ information reflecting the programming requirements for a general area of applications; programming content which reflects application requirements and hardware characteristics; and coprocessor specific hardware availability.

8. (Currently amended) A method for programming an accelerating coprocessor comprising the steps of:

accessing data reflective of programming requirements for a general area of applications; and

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identifying bit demands for the accelerating coprocessor acceleration function such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives.

9. (Currently amended) The method for programming an accelerating coprocessor of claim 8 comprising the ~~steps~~ step of:

accessing data reflective of programming content which reflects application requirements and hardware characteristics.

10. (Currently amended) The method for programming an accelerating coprocessor of claim 8 comprising the ~~steps~~ step of:

accessing data reflective of coprocessor specific hardware availability.

11. (Currently amended) The method of claim 8 further comprising the ~~steps~~ step of:

permitting an application trained non circuit design trained user to enter instructions to achieve accelerated performance.

12. (Currently amended) The method of claim 8 further comprising the ~~steps~~ step of:

creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

13. (Currently Amended) The method of claim 8 further comprising the ~~steps~~ step of:

~~identifying bit demands for the application specific coprocessor acceleration function, means for~~ identifying ~~correlating~~ resources available and needed for the coprocessor to provide application specific accelerated processing.

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14. (Currently amended) The method of claim 8 further comprising the ~~steps~~ step of:

identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

15. Canceled

16. (Currently amended) A method of compiling data for programming an accelerating coprocessor comprising the steps of:

creating an internal representation reflecting the operational characteristics of ~~a~~ the coprocessor corresponding to application specific accelerated processing needs~~, means for~~ ; and

identifying bit demands for the application specific ~~coprocessor acceleration function~~accelerated processing needs such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives.

17-20. Canceled

21. (Currently amended) A compiler for programming an accelerating coprocessor comprising:

means for accessing data reflective of programming requirements for a general area of applications; and

means for identifying bit demands for the accelerating coprocessor such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives.

22. (Original) The compiler for programming an accelerating coprocessor of claim 21 further comprising:

means for accessing data reflective of programming content which reflects application requirements and hardware characteristics.

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23. (Original) The compiler for programming an accelerating coprocessor of claim 21 further comprising:

means for accessing data reflective of coprocessor specific hardware availability.

24. (Previously presented) The compiler of claim 21 further comprising:

means for permitting an application trained non circuit design trained user to enter instructions to achieve accelerated performance.

25. (Previously presented) The compiler of claim 21 further comprising:

means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

26. Canceled

27. (Previously presented) The compiler of claim 21 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing.

28. (Previously presented) The compiler of claim 21 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

29. Canceled

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30. (Currently amended) A compiler for data for programming an accelerating coprocessor comprising:

means for creating an internal representation reflecting the operational characteristics of ~~a~~ the accelerating coprocessor corresponding to application specific accelerated processing ~~needs, means~~ needs; and

means for identifying bit demands for the application specific ~~coprocessor acceleration function~~accelerated processing such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives.

31-35. Canceled

36. (Currently amended) The method of claim 10 further comprising the ~~steps~~ step of:

permitting an application trained non circuit design trained user to enter instructions to achieve accelerated performance.

37. (Currently amended) The method of claim 36 further comprising the ~~steps~~ step of:

creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

38. Canceled

39. (Currently amended) The method of ~~claim 38~~ claim 37 further comprising the ~~steps~~ step of:

identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

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40. (Currently amended) The method of claim 11 further comprising the ~~steps~~ step of:

creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

41. Canceled

42. (Currently amended) The method of ~~claim 41~~ claim 40 further comprising the ~~steps~~ step of:

identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

43. Canceled

44. (Currently amended) The method of ~~claim 43~~ claim 12 further comprising the ~~steps~~ step of:

identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

45. Canceled

46. (Original) The compiler of claim 23 further comprising:

means for permitting an application trained non circuit design trained user to enter instructions to achieve accelerated performance.

47. (Original) The compiler of claim 46 further comprising:

means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

48. Canceled

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49. (Currently amended) The compiler of ~~claim 48~~ claim 47 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing.

50. (Original) The compiler of claim 49 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

51. (Original) The compiler of claim 24 further comprising:

means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs.

52. Canceled

53. (Currently amended) The compiler of ~~claim 52~~ claim 51 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing.

54. (Original) The compiler of claim 53 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

55. Canceled

56. (Currently amended) The compiler of ~~claim 55~~ claim 25 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing.

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57. (Original) The compiler of claim 56 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

58. (Currently amended) The compiler of ~~claim 26~~ claim 21 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing.

59. (Original) The compiler of claim 58 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

60. (Original) The compiler of claim 27 further comprising:

means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration.

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